WHAT IS CLAIMED IS:

1. A method of manufacturing a semiconductor device, the method comprising:

forming a first dielectric layer (30) overlying a substrate (10);

forming a first barrier layer (31), comprising a first dielectric barrier material, on the first dielectric layer (30);

etching to form a first opening (32) defined by side surfaces (30A) of the first dielectric layer (30) and a bottom;

forming a second barrier layer (40), comprising a second dielectric barrier material different from the first dielectric barrier material (31), on an upper surface of the first barrier layer overlying the first dielectric layer (30), on the side surfaces of the first dielectric layer defining the first opening and on the bottom of the opening;

etching, with selectivity to the first barrier layer, to remove the second barrier layer from, and stopping on, the upper surface of the first barrier layer, and to remove the second barrier layer from the bottom of the first opening, leaving a portion of the second barrier layer as a liner (50) on the side surfaces (30A) of the first dielectric layer (30) defining the first opening (32); and

filling the opening with metal to form a lower metal feature (60).

2. The method according to claim 1, wherein the first (31) and second (40) dielectric barrier materials are selected from the group consisting of silicon nitride, silicon oxynitride and silicon carbide, the method comprising depositing each of the first and second barrier layers by chemical vapor deposition.

3. The method according to claim 1, comprising filling the opening (32) with copper (Cu) or a Cu alloy (60).

4. The method according to claim 1, further comprising:

forming a third barrier layer (70), comprising a third dielectric barrier material different from the first dielectric barrier material, on the first barrier layer (31) and on an upper surface of the lower metal feature (60);

forming a second dielectric layer (71) on the third barrier layer (70);

forming a fourth barrier layer (72), comprising a fourth dielectric barrier material, on the second dielectric layer (71);

forming a third dielectric layer (73) on the fourth barrier layer (72);

forming a fifth barrier layer (74), comprising a fifth dielectric barrier material, on the third dielectric layer (73);

etching to form a dual damascene opening comprising an upper trench portion (76) defined by side surfaces (73A) of the third dielectric layer (73) in communication with a lower via hole (75) defined by side surfaces (71A) of the second dielectric layer (71) and a bottom on at least a portion of the upper surface of the lower metal feature (60);

forming a sixth barrier layer (80), comprising a sixth dielectric barrier material different from the first (31), fourth (72) and fifth (74) dielectric materials, on the fifth barrier layer (74) overlying the third dielectric layer (73), on the side surfaces (73A) of the third dielectric layer defining the trench (76), on the side surfaces (71A) of the second dielectric layer (71) defining the via hole (75), on a portion of the fourth barrier layer (72) between the trench (76) and via hole (75), and at the bottom of the via hole;

etching to remove the sixth barrier layer from, and stopping on, the fifth barrier layer, from and stopping on the fourth barrier layer, and at the bottom of the via hole, leaving a portion of the sixth barrier layer as a liner (91, 90) on the side surfaces (73A) of the third dielectric layer (73) defining the trench and on the side surfaces (71A) of the second dielectric layer (71) defining the via hole (75); and

filling the dual damascene opening with metal to form a metal line (100B) connected to an underlying metal via (100A).

5. The method according to claim 4, comprising filling the dual damascene opening with copper (Cu) or a Cu alloy (10C) to form a Cu or Cu alloy line (100B) connected to a Cu or Cu via (100A) which is electrically connected to the lower metal feature (60).

6. The method according to claim 4, further comprising depositing a seventh barrier layer (101), comprising a seventh dielectric barrier material, on an upper surface of the sixth barrier layer (74) and on an upper surface of the metal line (100B).

7. A semiconductor device comprising:

a lower metal feature (60), comprising copper (Cu) or a Cu alloy, formed in an opening defined by side surfaces (30A) of a first dielectric layer (30) having a first barrier layer (31), comprising a first dielectric barrier material, thereon;

a first barrier liner (50), comprising a second dielectric barrier material different from the first dielectric barrier material (31), on the side surfaces (30A) of the first dielectric layer (30) between the lower metal feature (60) and the first dielectric layer (30), the

first barrier liner (50) having an upper surface extending to a distance below an upper surface of the first dielectric layer (30).

8. The semiconductor device according to claim 7, further comprising:

a second barrier layer (70), comprising a third dielectric barrier material different from the first dielectric barrier material, on the first barrier layer (31) overlying the first dielectric layer (30); and

a dual damascene structure formed on and electrically connected to the lower metal feature (60), the dual damascene structure comprising:

a second dielectric layer (71) on the second barrier layer (70);

a third barrier layer (72), comprising a fourth dielectric barrier material, on the second dielectric layer (71);

a third dielectric layer (73) on the third barrier layer (72);

a fourth barrier layer (74), comprising a fifth dielectric barrier layer material, on the third dielectric layer (73);

a dual damascene opening comprising a trench (76), defined by side surfaces (73A) of the third dielectric layer (73), connected to a via hole (75), defined by side surfaces (71A) of the second dielectric layer (71) and a bottom on at least a portion of the upper surface of the lower metal feature (60);

a second barrier liner (90,91), comprising a sixth dielectric barrier material different from the first, fourth and fifth dielectric barrier materials, on the side surfaces (71A) of the second dielectric layer (71) defining the via hole (75) and on the side surfaces (73A) of the third dielectric layer (73) defining the trench (76); and

Cu or a Cu alloy (100) filling the dual damascene opening and forming a Cu or Cu alloy line (100B) in the third dielectric layer (73) connected to a via (100A) in the second dielectric layer (71) which, in turn, is electrically connected to the lower metal feature (60).

9. The semiconductor device according to claim 8, wherein:

an upper surface of the second barrier liner (90) on the side surfaces (71A) of the second dielectric layer (71) extends to a distance below the upper surface of the third barrier layer (72); and

an upper surface of the second barrier liner (91) on the side surfaces (73A) of the third dielectric layer (73) extends to a distance below the upper surface of the fourth barrier layer (74).

10. The semiconductor device according to claim 8, wherein the first (30), second (50), third (70), fourth (72), fifth (74) and sixth dielectric barrier (90, 91) materials are selected from the group consisting of silicon nitride, silicon carbide and silicon oxynitride.